WHAT IS CLAIMED IS:

1. A radially distributed serial control bus architecture, comprising:

a controller;

a plurality of connections, each connection having a first end and a second end, each of said first end of said each connection coupled to said controller; and

a plurality of peripheral cards each peripheral card individually coupled to a second end of a respective dedicated one of said plurality of connections.

2. The architecture of claim 1 wherein each of said peripheral cards includes a transmit connection and a collision connection, and further, wherein each of said transmit and collision connections for said each peripheral cards are connected to a separate second end of said respective dedicated one of said plurality of connections.

3. The architecture of claim 1 wherein each of said peripheral cards includes a transmit lead and a collision lead, and each of said transmit lead and said collision lead are separately coupled to said second end of said respective dedicated one of said plurality of connections.

4. The architecture of claim 1 further including a logic device provided between each of said peripheral cards and said controller.

5. The architecture of claim 4 wherein said logic device includes a field programmable gate array device.

6. The architecture of claim 4 wherein said logic device includes a plurality of drivers each dedicated to receive signals from a particular one of said plurality of peripheral cards, wherein said controller is configured to individually disable one or more of said plurality of drivers.

7. The architecture of claim 4 wherein said logic device includes:

a control unit for generating a control signal;

a plurality of OR gates each configured to perform an OR operation to said control signal and a signal received from a respective peripheral card; and

an AND gate configured to perform an AND operation to outputs of said OR gates, and to provide an output AND signal to said controller.

8. The architecture of claim 1 wherein each of said plurality of connections is a hard wire connection.

9. The architecture of claim 1 wherein said controller is one of a MPC 860 processor, a MPC 850 processor, and a MPC 8260 processor.

10. The architecture of claim 1 wherein said serial control bus is configured to operate at a frequency range between approximately 3 MHz and 6 MHz.

11. The architecture of claim 1 wherein each of said plurality of peripheral cards is separated from said system controller by a distance ranging from approximately one inch to seven feet.

12. The architecture of claim 1 wherein each of said plurality of peripheral cards are coupled to an optical data communications network, each configured to receive and transmit electrical and optical signals.

13. The architecture of claim 12 wherein said optical signals include one of OC-3, OC-12 and OC-48, and said electrical signals include one of STS-3, STS-12 and STS-48.

14. The architecture of claim 1 wherein said serial control bus may be configured to support a bandwidth of approximately 6 Mbps.

15. The architecture of claim 1 wherein said serial control bus may be configured to support half duplex mode and full duplex mode communication.

16. A method of providing a radially distributed serial control bus architecture, comprising the steps of:

connecting each of a first end of a plurality of connections to a controller; and

individually connecting each of a plurality of peripheral cards to a second end of a respective dedicated one of said plurality of connections.

17. The method of claim 16 wherein said step of individually connecting includes the step of separately connecting a transmit connection and a collision connection of each of said peripheral cards to said second end of said respective dedicated one of said plurality of connections.

18. The method of claim 16 wherein said step of individually connecting includes the step of individually coupling a transmit lead and a collision lead of each of said peripheral cards to said second end of said respective dedicated one of said plurality of connections.

19. The method of claim 16 further including the step of providing a logic device between each of said peripheral cards and said controller.

20. The method of claim 16 wherein said logic device includes a field programmable gate array device.

21. The method of claim 16 wherein said step of providing said logic device includes the steps of:

providing a plurality of drivers each dedicated to receive signals from a particular one of said plurality of peripheral cards; and

configuring said controller to individually disable one or more of said

plurality of drivers.

22. The method of claim 21 wherein said step of providing said logic device includes the step of:

generating a control signal;

performing an OR operation to said control signal and a signal received from each peripheral card; and

performing an AND operation to outputs of said OR operations and generating an output AND signal..

23. The method of claim 16 wherein each of said plurality of connections is a hard wire connection.

24. The method of claim 16 wherein said controller is one of a MPC 860 processor, a MPC 850 processor, and a MPC 8260 processor.

25. The method of claim 16 wherein said serial control bus is configured to operate at a frequency range between approximately 3 MHz and 6 MHz.

26. The method of claim 16 wherein each of said plurality of connections is approximately one inch to seven feet in length.

27. The method of claim 16 further including the step of coupling each of said plurality of peripheral cards to an optical data communications network, and configuring said each peripheral card to receive and transmit electrical and optical signals.

28. The method of claim 27 wherein said optical signals include one of OC-3, OC-12 and OC-48, and said electrical signals include one of STS-3, STS-12 and STS-48.

29. The method of claim 16 wherein said serial control bus may be configured to support a bandwidth of approximately 6 Mbps.

30. The method of claim 16 wherein said serial control bus may be configured to support half duplex mode and full duplex mode communication.

31. A method of fault isolation in a serial control bus architecture, comprising the steps of:

detecting a signal communication failure on a data control bus;

performing a control bus integrity check; and

isolating the origin of said signal communication failure on said bus to a particular peripheral device.

32. The method of claim 31 wherein said communication failure includes a peripheral card lack of response to a system controller request or a background poll.

33. The method of claim 31 wherein said step of performing said bus integrity check includes the steps of:

detecting a combined control bus signal; and

determining whether a transmit signal from a peripheral device is continuously low.